Remarks

Claims 1-20 are pending in this application. Reconsideration and allowance of the application are respectfully requested.

The instant Office Action dated July 31, 2007 indicated an objection to the drawings and also indicated that claims 1, 3-5 and 7-13 stand rejected under 35 U.S.C. 102(b) over Long (U.S. Patent No. 5,164,725). The examiner notes that claims 2 and 6 are objected to as being dependent on a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Applicant traverses the objection to the drawings based upon the drawings allegedly failing to show features of claims 11-13 as described in the specification. According to M.P.E.P. § 608.02(d), as noted in the Office Action, "Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing." Applicant submits that the limitations of claims 11-13 would be clear to one of skill in the art based upon Applicant's specification and Figures 1-2. Thus, any features of claims 11-13 that are not shown in the drawings do not need to be shown because it is not "essential for a proper understanding of the disclosed invention." Therefore, Applicant requests that the objection to the drawings be removed.

Applicant respectfully submits that the Section 102(b) rejection of claims 1, 3-5 and 7-13 cannot stand because the cited portions of the Long reference do not correspond to the claimed invention which includes, for example, aspects directed to the influences on the common line caused by the switches switching occurring at substantially regular intervals. The cited portions of Long teach that the gates of output FETs M3 and M5 are connected together to selection line 15 (*i.e.,* they both switch on/off together in response to a signal applied via selection line 15), thereby causing current sources M1 and M2 to turn on (and off) together. *See, e.g.,* Figure 2 and Col. 3:28-49. Long further teaches that the influences on common line V_{DD} caused by FETs M3 and M5 switching occur in response to the signal applied via selection line 15, not at substantially regular intervals as in the claimed invention. By way of example, claim 2 indicates that one and only one of the first and second switches switch each clock cycle, whereas Long's FETs M3 and M5 switch

together. Accordingly, Applicant requests that the Section 102(b) rejection of claims 1, 3-5 and 7-13 be withdrawn.

In response to the potential allowability of claim 2, Applicant has rewritten claim 2 in independent form as claim 14, including limitations believed to form the basis for the allowability of claim 2. Applicant submits that, as is consistent with the instant Office Action, claim 14, as well as claims 15-20 that depend from claim 14, are in condition for allowance over the cited references. Thus, Applicant requests that claims 14-20 be allowed.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131

CUSTOMER NO. 65913

By: _____
Name: Robert J. Crawford
Reg. No.: 32,122
651-686-6633 x2300
(NXPS.300PA)